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J Stark, MD Brown, YN Patt - Proceedings of the 33rd annual ACM/IEEE international ..., 2000 - portal.acm.org
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Global **instruction scheduling** for superscalar machines
D Bernstein, M Rodeh - Proceedings of the ACM SIGPLAN 1991 conference on ..., 1991 - portal.acm.org
... is no problem to activate the **instruction scheduling** after the register allocation is completed. 2 3 More precisely, usually the three cycle **delay** between a ...
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A Yoaz, M Erez, R Ronen, S Jourdan - ACM SIGARCH Computer Architecture News, 1999 - portal.acm.org
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Select-Free **Instruction Scheduling** Logic - all 18 versions »
M Brown, J Stark, Y Patt - Proceedings of the 34th Annual International Symposium on ..., 2001 - doi.ieeecomputersociety.org
... The need to prioritize all ready **instructions** adds to the **delay** in the **scheduling** loop; by removing the priori- tization and performing selection in a ...
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... par- allelism. In processors with hardware support for dynamic code **scheduling**, the scope of **instruction scheduling** is lim- ited ...
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D Ernst, A Hamel, T Austin - Computer Architecture, 2003. Proceedings. 30th Annual ..., 2003 - ieeexplore.ieee.org
... with each store set identifier the **delay** until the ... When **scheduling** stores, the latency of a store operation ... a store value to a load **instruction**, typically the ...
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